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JOINT INDUSTRY STANDARD

Space Applications Electronic Hardware Addendum to J-STD-001D Requirements for Soldered Electrical and Electronic Assemblies





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- Focus on end product performance
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- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

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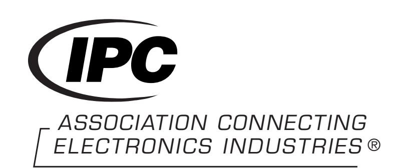
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J-STD-001DS

Space Applications Electronic Hardware Addendum to J-STD-001D Requirements for Soldered Electrical and Electronic Assemblies

Developed by the Space Electronic Assemblies J-STD-001 Addendum Task Group (5-22as) of the Assembly & Joining Processes Committee (5-20) of IPC

Users of this publication are encouraged to participate in the development of future revisions.

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Acknowledgment

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Space Applications Electronic Hardware Addendum to J-STD-001D Requirements for Soldered Electrical and Electronic Assemblies

1 SCOPE

This addendum provides additional requirements over those published in IPC J-STD-001D to ensure the reliability of soldered electrical and electronic assemblies that must survive the vibration and thermal cyclic environments getting to and operating in space.

1.1 Purpose When required by procurement documentation/drawings, this Addendum supplements or replaces specifically identified requirements of IPC/EIA J-STD-001, Revision D of February 2005.

1.2 Precedence The contract takes precedence over this Addendum, referenced standards and user-approved drawings (see IPC J-STD-001D 1.7.1). In the event of a conflict between this Addendum and the applicable documents cited herein, this Addendum takes precedence. Where referenced criteria of this addendum differ from the published IPC J-STD-001D, this addendum takes precedence.

1.3 Existing or Previously Approved Designs This Addendum **shall not** constitute the sole cause for the redesign of previously approved designs. When drawings for existing or previously approved designs undergo revision, they should be reviewed and changes made that allow for compliance with the requirements of this Addendum.

1.4 Use This addendum is not to be used as a stand-alone document.

Where criteria are not supplemented, the Class 3 requirements of IPC J-STD-001D apply. If an IPC J-STD-001D requirement is changed or added by this Addendum, the clause is identified and the entire IPC J-STD-001D clause is replaced by this addendum.

The clauses modified by this Addendum do not include subordinate clauses unless specifically stated (e.g., 1.4 does not include 1.4.1). Clauses, Tables, Figures, etc., in IPC J-STD-001D that are not listed in this addendum are to be used as-published.

A description of the change is provided to describe the difference from the original requirement, and in most cases, an explanation for the change is provided.

1.5 Reduction of Hazardous Substances (RoHS)

1.5.1 Impact Mitigation Components, subassemblies, assemblies and hardware **shall** be screened to limit the incorporation of lead-free (LF) technology into electrical/electronic equipment for space flight applications.

Electrical/electronic components identified as having external surfaces, platings, metallization, etc., with a lead-free (LF) finish **shall** require the retinning of all exposed LF surfaces, platings, metallization, etc., with tin-lead (SnPb) solder with a lead (Pb) alloy of 3% minimum, or **shall** be fully protected to mitigate metallic whisker formation in the expected end-use application/environment. Retinning **shall not** degrade or damage the component.

Subassemblies, assemblies and mounting hardware identified as having LF surfaces, platings, metallization, etc., **shall** be protected by process or design to mitigate metallic whisker formation in the expected end-use application/environment.

Lead-free (LF) solder alloys (< Pb03) **shall not** be used in the manufacture of spaceflight and other mission-critical hardware.

1.5.2 Tin Whisker Mitigation Electrical/electronic components identified as having conductor platings, metallization, etc., with a lead-free (LF) finish **shall** require the retinning of all exposed LF surfaces, platings, metallization, etc., with tin-lead (SnPb) solder alloy covering all exposed surfaces of the lead-free plated conductors up to the body-lead seal. The process **shall** be repeatable, controlled, not introduce immediate or latent damage, or degrade the performance of the component. The retinning requirement applies to all components (surface mount and through-hole).

The following requirements are applicable:

1. SnPb pretinning on RoHS compliant components (exhibiting a lead-free finish) must cover all exposed surfaces of the conductors with a tin-lead (SnPb) alloy. This will involve immersion plating up to the body lead seal, and will require verification that the process is controlled and does not introduce immediate or latent damage, or degrade the performance of the component.
2. Solder immersion of conductors **shall not** exceed 5 seconds duration maximum. Duration of molten solder contact with the body-lead seal **shall not** exceed 2 seconds.

J-STD-001DS Table 1 Space Applications Requirements

J001D Reference	Space Applications Requirement (as changed by this Addendum)	Description of Change
1.5	**Definition of Requirements** When the word ‘‘**shall**‘‘ is used in this document, it expresses a requirement that is mandatory. Where the word ‘‘**shall**‘‘ leads to a hardware defect for at least one class, the requirements for each class are annotated in text boxes located adjacent to that occurrence in the text. These boxes are summarized in Appendix A. In case of a discrepancy between requirements in the text boxes and Appendix A, requirements listed in the text boxes take precedence. Line drawings and illustrations are depicted herein to assist in the interpretation of the written requirements of this standard. Text takes precedence over the figures. IPC-HDBK-001, a companion document to this specification, contains valuable explanatory and tutorial information compiled by IPC Technical Committees that is relative to this specification. Although the Handbook is not a part of this specification, when there is confusion over the specification verbiage, the reader is referred to the Handbook for assistance.	The first paragraph is reworded so that wherever the word ‘‘**shall**‘‘ is used, it expresses a requirement that is mandatory.
1.5.1	**Hardware Defects** Hardware characteristics or conditions that do not conform to the requirements of this specification that are detectable by inspection or analysis **shall** be classified as hardware defects. Hardware defects **shall** be identified and **shall** be dispositioned, e.g., rework, scrap, use as is, or repair. It is the responsibility of the user (see 1.8.13) to define additional or unique defect categories applicable to the product. It is the responsibility of the manufacturer (see 1.8.5) to identify defects that are unique to the assembly process (see 1.13.2).	Clause renamed to remove reference to Process Indicators. This Addendum does not rewrite every clause in the standard for the purpose of removing text boxes. As stated in this Addendum Clause 1.5, nonconformance to the word **shall** is always a defect and text boxes should be ignored.
1.6	**General Requirements** Surface mount designs need to undergo ‘Design for Reliability’ procedures based on the design parameters, the use conditions, the design life, and the acceptable failure risk to assure the designs capability to reliably function for its intended use. For ‘‘Design for Reliability’’ information see IPC-D-279 and IPC-9701. The soldering operations, equipment, and conditions described in this document are based on electrical/ electronic circuits designed and fabricated in accordance with the specifications listed in Table 1-1.	The first paragraph was deleted because it discusses agreement on product class. 1.4 states that when criteria are not supplemented, the Class 3 requirements of J-STD-001D apply.
1.10	**Personnel Proficiency** All instructors, operators, and inspection personnel **shall** be proficient in the tasks to be performed. Objective evidence of that proficiency **shall** be maintained and be available for review. Objective evidence should include records of training to the applicable job functions being performed, work experience, testing to the requirements of this standard, and/or results of periodic reviews of proficiency. Training **shall** be in accordance with the IPC J-STD-001D Training and Certification Program, with the addition of Module 6, Space Requirements for Soldered Electronic Assemblies. All training **shall** be traceable to a Master IPC Trainer (MIT).	The last sentence of the published IPC J-STD-001D paragraph was deleted to disallow supervised on the job training for fabricating space hardware. A new second paragraph was added requiring structured training in a classroom-type environment that is traceable to an IPC J-STD-001 MIT.
1.11	**Acceptance Requirements** All products **shall** meet the requirements of the assembly drawing(s)/documentation and the requirements specified herein. Manufacturers **shall** perform 100% inspection using either visual inspection or a nondestructive evaluation. Nondestructive verification techniques **shall** be approved by the User prior to use.	‘‘for the applicable product class’’ was deleted from the first sentence because it references different product classes. 1.4 states that when criteria are not supplemented, the Class 3 requirements of J-STD-001D apply. The second paragraph and its bullets were replaced to require 100% inspection on all products and that NDE methods are approved by the User prior to use.

J001D Reference	Space Applications Requirement (as changed by this Addendum)	Description of Change
1.13.2.2	**High Frequency Applications** High frequency applications (i.e., radio wave and microwaves) may require part clearances, mounting systems, and assembly designs which vary from the requirements stated herein. When high frequency design requirements prevent compliance with the design and part mounting requirements contained herein, manufacturers may use alternative designs. Alternative designs, including acceptance criteria **shall** be approved by the User prior to use.	Added requirement for User approval of alternative designs and criteria prior to use. These are unique topics that require unique processes. It is important to know how the manufacturer intends to manufacture these types of products in order to assure personnel and/or hardware safety, and that the alternate designs will survive space environments.
1.13.2.3	**High Voltage Applications** High power applications may require part clearances, mounting systems, and assembly designs which vary from the requirements stated herein. When such design requirements prevent compliance with the design and part mounting requirements contained herein, manufacturers may use alternative designs. Alternative designs, including acceptance criteria **shall** be approved by the User prior to use.	Added requirement for User approval of alternative designs and criteria prior to use. These are unique topics that require unique processes. It is important to know how the manufacturer intends to manufacture these types of products in order to assure personnel and/or hardware safety, and that the alternate designs will survive space environments. The reference to broken strands in J-STD-001D was deleted because this Addendum does not permit broken strands for any reason.
3.1	**Materials** The materials and processes used to assemble/manufacture electronic assemblies **shall** be selected such that their use, in combination, produce products acceptable to this standard. When major elements of the proven processes are changed (e.g., flux, solder paste, cleaning media or system, solder alloy or soldering system), validation of the acceptability of the change(s) **shall** be performed and documented in accordance with Appendix C or other approved tests agreed upon between the manufacturer and user, and approved by the user prior to use. Major elements may also pertain to a change in bare board supplier, solder resist, or metallization. Limited shelf life items **shall** be stored and controlled in accordance with material manufacturer's recommendations or in accordance with the manufacturer's documented procedures for controlling shelf life and shelf life extensions that may be permitted.	These three paragraphs replace J-STD-001D Clause 3.1. Since changes to major elements of a process can affect reliability, the 3rd sentence was reworded to make it a requirement that any major changes to proven processes are validated and approved by the User prior to use. The last sentence was added to ensure control over limited shelf life items.
3.2	**Solder** Solder **shall** be in accordance with J-STD-006 or equivalent. High temperature solder alloys, e.g., Sn96, **shall** only be used where specifically indicated by approved drawings. Solder alloys other than Sn60A, Pb36B, and Sn63A that provide the service life, performance, and reliability required of the product may be used if all other conditions of this standard are met and objective evidence of such is reviewed and approved by the User prior to use. Flux that is part of flux-cored solder wire **shall** meet the requirements of 3.3. Flux percentage is optional.	Reworded to require that the compatibility of alternate solder alloys be substantiated, with data, to ensure the performance of the alternate solder alloy for the expected environment and is approved by the User prior to use. Also, high-temperature alloys such as Sn96 can only be used where specifically required.
3.3	**Flux** Flux **shall** be in accordance with J-STD-004 or equivalent. Flux **shall** conform to flux activity levels L0 or L1 of flux materials rosin (RO) or resin (RE). When other activity levels or flux materials are used, data demonstrating compliance with testing of Appendix C or other approved tests agreed upon between the manufacturer and user **shall** be approved by the User prior to use. **Note:** Flux or solder paste soldering process combinations previously tested or qualified in accordance with other specifications do not require additional testing. Type H or M fluxes **shall not** be used for tinning of insulated wires except for solid wires with insulation bonded to the wire, e.g., magnet wire. For all fluxing applications where adequate cleaning is not practical, only flux types RO or RE of the L0 flux activity level, or equivalent, **shall** be used.	First sentence was reworded to remove the allowance for using fluxes other than those shown on space hardware without prior User approval. Reworded the end of the sentence to require User approval, prior to use, for higher activity level fluxes which can leave residues that can lead to corrosion or conductive growth.
3.7	**Chemical Strippers** Chemical solutions, pastes, and creams used to strip solid wires **shall not** cause degradation to the wire. Chemical strippers **shall not** be used with stranded wires. Chemical stripping materials **shall** be completely neutralized and be cleaned such that there are no residues from the stripping, neutralizing, or cleaning steps.	A new last sentence was added to ensure there are no residues from the stripping or cleaning processes.

J001D Reference	Space Applications Requirement (as changed by this Addendum)	Description of Change
3.9	**Components** Components (e.g., electronic devices, mechanical parts, and printed boards) selected for assembly **shall** be compatible with all materials and processes, e.g., temperature ratings, used to manufacture the assembly/product. Moisture sensitive components (as classified by IPC/JEDEC J-STD-020 or other documented classification procedure) **shall** be handled in a manner consistent with IPC/JEDEC J-STD-033 or other documented procedure. During tinning of leads, heat sinks **shall** be attached to the leads of components that are heat sensitive. If it is not possible to implement an effective heat sink, the component **shall** be preheated.	Added the third paragraph to ensure heat sensitive components are protected during the manufacturing process.
3.9.3	**Gold Removal** Regardless of thickness, gold **shall** be removed: • From at least 95% of the surface to-be-soldered of the through-hole component leads. • From 95% of all surfaces of surface mount components to-be-soldered regardless of gold thickness. • From the to-be-soldered surface of solder terminals. • A double tinning process or dynamic solder wave may be used for gold removal. Electroless nickel immersion gold (ENIG) finishes on PCBs are exempt from this requirement. These requirements may be eliminated if there is documented objective evidence available for review that there are no gold related solder embrittlement problems associated with the soldering process being used.	To address concerns over gold embrittlement, the first bullet was reworded to remove the allowance for soldering to gold thicknesses of less than 2.5 µm [0.0984 mil]. The third bullet was reworded to include the words ''to-be-soldered'' to clarify that the entire terminal does not need the gold removed; and to remove the allowance for soldering to gold thicknesses of less than 2.5 µm [0.0984 mil].
3.9.4	**3.9.4 Rework of Nonsolderable Parts** A component lead, termination, or board not conforming to the solderability requirements of 3.9.1 may be reworked (e.g., by dipping in hot solder) before soldering. A reworked part **shall** conform to the requirements of 3.9.1, less steam conditioning.	Reference to heat sinks was deleted; this is covered in the parent clause 3.9.
3.11	**Soldering Tools and Equipment** Tools and equipment **shall** be selected, used, and maintained such that no damage or degradation that would be detrimental to the designed function of parts or assemblies results from their use. Soldering irons, equipment, and systems **shall** be chosen and employed to provide temperature control and isolation from electrical overstress or ESD (see 4.1), and be calibrated in accordance with ISO 17025 or ANSI/NCSL-Z540- 1-1994. A tool used to cut leads **shall not** impart shock that damages a component lead seal or internal connection. See Appendix B for guidelines on tool selection and maintenance.	The word ''used'' was moved to make a requirement that the right tools are used and that they are used as they are intended to be and added a requirement for calibration. Calibration to a known standard is a vital control in the manufacture of space hardware (although recommended in Appendix B, the appendices in IPC J-STD-001D are informational and are not considered requirements unless otherwise specified).
4.3	**General Part Mounting Requirements** When design restrictions mandate mounting components incapable of withstanding soldering temperatures incident to a particular process, such components **shall** be mounted and soldered to the assembly using a process compatible with the part to be soldered. Parts **shall** be mounted with sufficient clearances between the body and the PCB to assure adequate cleaning and cleanliness testing. Assemblies should be cleaned after each soldering operation so that subsequent placement and soldering operations are not impaired by contamination (see 8, Cleaning Process Requirements). On assemblies using mixed component mounting technology, through-hole components should be mounted on one side of the printed board. Surface mounted components may be mounted on either or both sides of the assembly. Where component marking visibility and legibility is required, the contract or drawing **shall** so state. Parts should be mounted such that part markings and reference designators are visible.	Modified the end of the first paragraph to require that the process used in the ''separate operation'' does not harm the component(s). Deleted ''If cleaning is required'' from the start of the second paragraph because all hardware must be cleaned. Inserted a new first sentence in the fourth paragraph to require documentation on drawings when marking must be visible and legible.

<table>
<tr><th>J001D Reference</th><th>Space Applications Requirement (as changed by this Addendum)</th><th>Description of Change</th></tr>
<tr><td>4.9.3</td><td>Drying/Degassing Prior to soldering, the assembly shall be treated to remove detrimental moisture and other volatiles using a documented process.</td><td>This was changed from optional to a requirement because PCBs that are not demoisturized are susceptible to board damage and solder defects when exposed to soldering temperatures.</td></tr>
<tr><td>4.14.3</td><td>Solder Connection Defects The following solder joint conditions shall be considered defects:
a. Fractured solder connections.
b. Disturbed solder connections.
c. Cold solder connections.
d. Solder that violates minimum electrical clearance (e.g., bridges), or contacts the component body (except as noted in 7.6.7 and 7.6.8).
e. Fails to comply with wetting criteria of 4.14.
f. Solder bridging between joints except when path is present by design.
g. Overheated solder connection.
h. Blowholes, pinholes, and voids (where the bottom and all sides are not visible).
i. Excessive solder (solder in the bend radius of axial leaded parts in PTHs is not cause for rejection provided the lead is properly formed, the topside bend radius is discernible, and the solder does not extend to within 1 lead diameter of the part body or end seal).
j. Insufficient solder.
k. Rosin solder joint.
l. Contamination (e.g., lint, flux, dirt, extraneous solder/metal).</td><td>Items ''g'' through ''l'' were added to the originally published IPC J-STD-001D criteria for solder connection defects.</td></tr>
<tr><td>4.14.4</td><td>Partially Visible or Hidden Solder Connections Partially visible or hidden solder connections are acceptable provided that the following conditions are met:
a. The design does not restrict solder flow to any connection element on the solder destination side lands (e.g., PTH component) of the assembly.
b. The visible portion, if any, of the connection on either side of the PTH solder connection (or the visible portion of the SMD connection) is acceptable.
c. Process controls are maintained in a manner assuring repeatability of assembly techniques.
d. For solder connections that do not meet any of the above conditions, NDE shall be used. The User shall approve the NDE method prior to use.</td><td>Since all connections require inspection, ''d'' was added to require NDE if ''a'' through ''c'' cannot be met. The NDE method selected needs to be approved prior to use because the User may be more aware of potential damage to the assembly (e.g., maximum radiation levels the assembly can withstand).</td></tr>
<tr><td>5.1</td><td>Wire and Cable Preparation Insulation discoloration resulting from thermal stripping is permissible; however, the insulation shall not be charred. Chemical insulation stripping agents shall be used only for solid wire and are to be neutralized or removed prior to soldering (see 3.7 of this Addendum).

Table 5-1 does not apply; there shall be no nicked or broken wire strands. Exception: strand damage up to 10% deformation caused by nicks or scrapes is acceptable if the damage is fully encased in the solder connection. For plated wires, a visual anomaly that does not expose basis metal is not considered to be strand damage.

Birdcaging shall not extend beyond the insulation outside diameter. Wires that exhibit minor deformation shall comply with the deformation limits defined in paragraph 6.1.2 of this Addendum.</td><td>This was changed to disallow any severed strands; and to define deformation limits as those allowed for components in clause 6.1.2 of this Addendum.

Birdcaged, nicked, or gouged wires are easily broken and can result in conductive debris, open circuits, or electrical overstress (EOS) because of reduced wire size.</td></tr>
<tr><td>5.3.6</td><td>Table 5-2 Terminal Soldering Requirements
This replaces J-STD-001D Table 5-2.
<table><tr><th>Criteria</th><th>Space Reqmt.</th></tr><tr><td>A. Circumferential fillet and wetting - solder source side</td><td>360°</td></tr><tr><td>B. Percentage of solder source side land area covered with wetted solder</td><td>75%</td></tr></table></td><td>Feature A was changed from 330° to 360° to prevent flux entrapment, seal joints and minimize stresses around the joint.</td></tr>
</table>

<table>
<tr><th>J001D Reference</th><th>Space Applications Requirement (as changed by this Addendum)</th><th>Description of Change</th></tr>
<tr><td>6.1.1</td><td>Lead Forming Part and component leads should be preformed to the final configuration excluding the final clinch or retention bend before assembly or installation. The lead forming process shall not damage lead seals, welds, or connections internal to components. Leads shall not be reformed except for minor adjustments to bend angles.

Leads shall extend at least one lead diameter or thickness but not less than 0.8 mm [0.031 in] from the body or weld before the start of the bend radius (see Figure 6-1).

The lead bend radius shall be in accordance with Table 6-1.

Note: Measurement is made from the end of the part. (The end of the part is defined to include any coating, solder seal, solder or weld bead, or any other extension.)

Table 6-1 Lead Bend Radius
<table>
<tr><th>Lead Diameter</th><th>Minimum Bend Radius (R)</th></tr>
<tr><td>Less than to 0.8 mm [0.031 in]</td><td>1 diameter/thickness</td></tr>
<tr><td>From 0.8 to 1.2 mm [0.031 to 0.047 in]</td><td>1.5 diameters/thickness</td></tr>
<tr><td>Greater than 1.2 mm [0.047 in]</td><td>2 diameters/thickness</td></tr>
</table></td><td>The last sentence of the first paragraph was added because lead forming cold works metals. Multiple forming can result in fatigue failure of the lead.</td></tr>
<tr><td>6.1.2</td><td>Lead Deformation Limits Whether leads are formed manually or by machine or die, parts or components shall not be mounted if the part or component lead has any nicks, scrapes or gouges. Exception: damage up to 10% deformation caused by nicks or scrapes are acceptable if the damage is fully encased in the solder connection. Smooth indentations up to 10%, e.g. tooling marks, and as allowed for intentionally flattened leads (see 7.1.4), of the diameter, width, or thickness of the lead are acceptable. Exposed basis metal is acceptable if deformation does not exceed the limits defined by this paragraph and does not impact solderability.</td><td>The first sentence was reworded to disallow ''nicks or deformation exceeding 10% of the diameter, width, or thickness of the lead...,'' and the last sentence was reworded to maintain continuity with the changed requirement in the first sentence.

Stresses are concentrated in the ''V'' of nicks, scrapes, or gouges. This type of damage, even if only 5% of the lead diameter have caused lead fracture during vibration testing.</td></tr>
<tr><td>6.1.3</td><td>Lead Termination Requirements Component leads in supported holes may be terminated using a straight through, partially clinched, or clinched configuration. The clinch should be sufficient to provide mechanical restraint during the soldering process. The orientation of the clinch relative to any conductor is optional. DIP leads should have at least two diagonally opposing leads partially bent outward.

Lead terminations in unsupported holes shall be clinched a minimum of 45°.

If a lead or wire is clinched, the lead shall be wetted in the clinched area. The outline of the lead should be discernible in the solder connection.

Tempered leads shall not be terminated with a (full) clinched configuration.

Lead protrusion shall not violate minimum electrical clearance requirements. Lead protrusion shall be in accordance with Table 6-2 for unsupported holes or Table 6-3 for supported holes.

Table 6-2 Protrusion of Leads in Unsupported Holes
<table>
<tr><td>(L) min.</td><td>Sufficient to clinch</td></tr>
<tr><td>(L) max. 1</td><td>No danger of shorts[2]</td></tr>
</table>
Note 1. Lead protrusion should not exceed 2.5 mm [0.0984 in] if there is a possibility of violation of minimum electrical spacing, damage to soldered connections due to lead deflection or penetration of static protective packaging during subsequent handling or operating environments.
Note 2. See 6.2.1.

Table 6-3 Protrusion of Leads in Supported Holes
<table>
<tr><td>(L) min.</td><td>End is discernible in solder[1]</td></tr>
<tr><td>(L) max.</td><td>2.25 mm [0.09 in]</td></tr>
</table>
Note 1. For boards greater than 2.3 mm [0.0986 in] thick, with components having pre-established lead lengths, e.g., DIPs, sockets, connectors, as a minimum need to be flush to the board surface, but may not be visible in the subsequent solder connection.

Connector, relay and tempered leads are exempt from the maximum length requirement provided that they do not violate minimum electrical spacing at the next higher assembly level.</td><td>Added new last paragraph exempting connector, relay, and tempered leads from protrusion limits.

Deleted note 2 from table 6-3 because it applied to Classes 1 and 2.</td></tr>
</table>

<table>
<tr><th>J001D Reference</th><th>Space Applications Requirement (as changed by this Addendum)</th><th>Description of Change</th></tr>
<tr><td>6.3.2</td><td>Table 6-5 This replaces J-STD-001D Table 6-5.
<table>
<tr><th></th><th>Criteria</th><th>Space Reqmt.</th></tr>
<tr><td>A.</td><td>Circumferential wetting on solder destination side of lead and barrel.</td><td>360°</td></tr>
<tr><td>B.</td><td>Vertical fill of solder. Note 2.</td><td>75%</td></tr>
<tr><td>C.</td><td>Circumferential fillet and wetting on solder source side of lead and barrel. Note 2.</td><td>360°</td></tr>
<tr><td>D.</td><td>Percentage of original land area covered with wetted solder on solder destination side. Note 3.</td><td>0</td></tr>
<tr><td>E.</td><td>Percentage of original land area covered with wetted solder on solder source side. Note 2.</td><td>75%</td></tr>
</table>
Note 1. Wetted solder refers to solder applied by any solder process including intrusive soldering.
Note 2. Applies to any side to which solder or solder paste was applied. The 25% unfilled height includes a sum of both source and destination side depressions.
Note 3. Provided the solder has flowed onto, and wetted to, the lead and solder pad before receding, and the recession or shrinkback cannot be construed to be a solder void or blowhole.</td><td>Features A and C were changed to require complete circumferential wetting. The lack of complete circumferential wetting around the lead, barrel, or pad indicates solderability problems that must be addressed. Notes 1 and 2, are the same as published in IPC J-STD-001D. Note 3 was modified to clarify. Note 4 was deleted because it applied to Class 2 only.</td></tr>
<tr><td>Table 7-1</td><td>Table 7-1 This replaces J-STD-001D Table 7-1.
<table>
<tr><td>A. Two lead widths for flat leads.</td></tr>
<tr><td>B. Two lead widths for coined leads.</td></tr>
<tr><td>C. Two lead diameters for round leads.</td></tr>
</table></td><td>Row A was increased to two lead widths. For severe operational environments, extra consideration should be given to maximize the minimum available contact length for A, B, & C.</td></tr>
<tr><td>7.1.1</td><td>Surface Mount Device Lead Deformation There shall be no unintentional lead deformation beyond the limits defined in Paragraph 6.1.2.</td><td>This entire clause (including subparagraphs a-e) is deleted and replaced with this Addendum requirement. Unintentional bending can affect stress relief and lead to fatigue fractures.</td></tr>
<tr><td>7.3</td><td>Leaded Component Body Positioning The maximum clearance between the bottom of a leaded component body and the printed wiring surface should be 2.0 mm [0.0787 in]. Parts insulated from circuitry or over surfaces without exposed circuitry may be mounted flush. Uninsulated parts mounted over exposed circuitry or which are in close proximity with other conductive materials shall be separated by suitable insulation.</td><td>The last sentence was reworded to require insulation of a suitable material because an air gap is not a suitable dielectric.</td></tr>
<tr><td>7.6.3</td><td>Table 7-3 This replaces J-STD-001D Table 7-3.
<table>
<tr><th>Feature</th><th>Dim.</th><th>Space Reqmt.</th></tr>
<tr><td>Maximum Side Overhang</td><td>A</td><td>25% (W) Note 1</td></tr>
<tr><td>End Overhang</td><td>B</td><td>Not permitted</td></tr>
<tr><td>Minimum End Joint Width</td><td>C</td><td>75% (W) or 75% (P), whichever is less</td></tr>
<tr><td>Minimum Side Joint Length</td><td>D</td><td>Note 3</td></tr>
<tr><td>Maximum Fillet Height</td><td>E</td><td>Note 3</td></tr>
<tr><td>Minimum Fillet Height</td><td>F</td><td>Note 3</td></tr>
<tr><td>Solder Thickness</td><td>G</td><td>Note 3</td></tr>
<tr><td>Minimum End Overlap</td><td>J</td><td>50% of component end termination metallization length</td></tr>
<tr><td>Termination Length</td><td>L</td><td>Note 2</td></tr>
<tr><td>Land Width</td><td>P</td><td>Note 2</td></tr>
<tr><td>Termination Width</td><td>W</td><td>Note 2</td></tr>
</table>
Note 1. Does not violate minimum electrical clearance.
Note 2. Unspecified parameter or variable in size, determined by design
Note 3. Wetting is evident.</td><td>Dimension A was changed to ensure at least 75% of the lead width is on the pad, and Dimension J was changed to ensure at least 50% of the lead length is on the pad.</td></tr>
</table>

<table>
<tr><th>J001D Reference</th><th>Space Applications Requirement (as changed by this Addendum)</th><th>Description of Change</th></tr>
<tr><td>7.6.6</td><td>Castellated Terminations
1. If parts with castellated terminations are chosen by design, their use shall be approved by the User. When used, the existing J-STD-001D Class 3 requirements apply.
2. Clarification of the relationship between Features D and G: If a part has bottom metallization, the minimum side joint length shown as Feature D becomes Feature G, the length of the bottom metallization.</td><td>1. Castellated part package types are not recommended for space applications. Coefficient of thermal expansion (CTE) mismatches between the part and the substrate can substantially reduce the life of the soldered connections.
2. Since the part chosen for Figure 7-6 does not have bottom metallization, it can be inferred that wetting of any bottom metallization to a land is not required. It is the intent of J-STD-001D that Feature G requires wetting to be evident between any bottom metallization and the land.</td></tr>
<tr><td>7.6.8</td><td>Table 7-8 This replaces J-STD-001D Table 7-8.
<table>
<tr><th>Feature</th><th>Dim.</th><th>Space Reqmt.</th></tr>
<tr><td>Maximum Side Overhang</td><td>A</td><td>25% (W) or 0.5 mm [0.02 in], whichever is less; Note 1</td></tr>
<tr><td>Maximum Toe Overhang</td><td>B</td><td>Note 1</td></tr>
<tr><td>Minimum End Joint Width</td><td>C</td><td>75% (W)</td></tr>
<tr><td>Minimum Side Joint Length</td><td>D</td><td>100% of available lead to land interface</td></tr>
<tr><td>Maximum Heel Fillet Height</td><td>E</td><td>Note 4</td></tr>
<tr><td>Minimum Heel Fillet Height</td><td>F</td><td>(G) + (T) Note 5</td></tr>
<tr><td>Solder Thickness</td><td>G</td><td>Note 3</td></tr>
<tr><td>Formed Foot Length</td><td>L</td><td>Note 2</td></tr>
<tr><td>Minimum Side Joint Height</td><td>Q</td><td>(G) + 50% (T)</td></tr>
<tr><td>Thickness of Lead at Joint Side</td><td>T</td><td>Note 2</td></tr>
<tr><td>Flattened Lead Width or Diameter of Round Lead</td><td>W</td><td>Note 2</td></tr>
</table>
Note 1. Does not violate minimum electrical clearance.
Note 2. Unspecified parameter or variable in size as determined by design.
Note 3. Wetting is evident.
Note 4. Solder fillet may extend through the top bend. Solder does not touch package body or end seal, except for plastic SOIC or SOT devices. Solder should not extend under the body of surface mount components whose leads are made of Alloy 42 or similar metals.
Note 5. In the case of a toe-down lead configuration, the minimum heel fillet height (F) extends at least to the mid-point of the outside lead bend.</td><td>Change Dim. D to 100% available lead/land interface to increase the strength of the connection.</td></tr>
</table>

<table>
<tr><th>J001D Reference</th><th>Space Applications Requirement (as changed by this Addendum)</th><th>Description of Change</th></tr>
<tr><td>7.6.14</td><td>

Surface Mount Area Array Packages These criteria are intended to apply to devices with solder balls that collapse during reflow. For devices where the balls are not expected to collapse or for devices using column grid arrays criteria **shall** be established and agreed upon between the manufacturer and user.

A BGA criterion defined herein assumes an inspection process is established to determine compliance using X-Ray and normal visual inspection processes. Visual inspection can be used to a limited extent, but evaluation of X-Ray images **shall** be used to allow assessment of characteristics that cannot be accomplished by normal visual means (e.g., misalignment, voids, missing balls).

Visual inspection requirements:

- When visual inspection is used, the magnification levels of Tables 11-1 and 11-2 apply.
- The solder terminations on the outside row (perimeter) of the BGA should be visually inspected whenever practical.
- The BGA needs to align in both X & Y directions with the corner markers on the PCB (if present).
- Absence of BGA solder ball(s) are defects unless specified by design.

Process development and control is essential for continued success of assembly methods and implementation of materials. BGA process guidance is provided in IPC-7095, which contains recommendations developed from extensive discussion of BGA process development issues.

Note: X-ray equipment not intended for electronic assemblies or not properly set up can damage sensitive components.

Surface mount area array packages **shall** meet the dimensional and solder fillet requirements of Table 7-14.

This replaces J-STD-001D Table 7-14.

Table 7-14 Dimensional Critera - Area Array/Ball Grid Array

<table>
<tr><th>Feature</th><th>Space Reqmt.</th></tr>
<tr><td>Alignment</td><td>Solder ball offset does not violate minimum electrical clearance.</td></tr>
<tr><td>Solder Ball Spacing, Figure 7-14</td><td>Solder ball offset (c) does not violate minimum electrical clearance.</td></tr>
<tr><td>Soldered Connection</td><td>a. Solder connections meet the criteria of 4.14.2
b. BGA solder balls contact and wet to the land forming a continuous elliptical round or pillar connection</td></tr>
<tr><td>Voids</td><td>25% or less voiding of any ball. Notes 1, 2</td></tr>
<tr><td>Under-fill or staking material</td><td>Required underfill or staking material is present and completely cured.</td></tr>
</table>

Note 1. Design induced voids, e.g., microvia in land, are excluded from this criteria. In such cases acceptance criteria will need to be established between the manufacturer and user.

Note 2. Manufacturers may use test or analysis to develop alternate acceptance criteria for voiding that consider the end-use environment.

</td><td>

The second sentence in the first paragraph was added to address technologies other than balls that are intended to collapse during reflow.

The second paragraph was reworded to require x-ray evaluation as part of the verification process.

The first bullet under ''Visual Inspection Requirements'' was reworded to clarify that visual inspection alone is not acceptable to verify product acceptance and to correct the incorrect reference to Table 11.2.2.1 in the published J-STD-001D (early printings).

The void requirement in Table 7-14 was reworded to ensure no one ball contains greater than a 25% void.

</td></tr>
</table>

J001D Reference	Space Applications Requirement (as changed by this Addendum)	Description of Change
8.3	**Post Solder Cleanliness** Visual inspection is used to assess the presence of foreign particulate matter as required in 8.3.1, or flux and other ionic or organic residues as required in 8.3.2 (see 11.2.2). Surfaces cleaned **shall** be inspected between 4X and 10X magnification and **shall** be free of visual evidence of residue or contaminants. Surfaces not cleaned may have evidence of flux residues.	The second paragraph was added to require visual inspection of cleaned surfaces to be performed at between 4X and 10X magnification. Many types of debris or contamination are hard to see without magnification, particularly when trying to see under quad-packs, DIPs, etc.
8.3.1	**Particulate Matter** Assemblies **shall** be free of dirt, lint, solder splash, dross, wire clippings, solder balls or other metal particles, etc. Solder balls are allowed if proven secured (i.e., will not come loose in operation of the system) with a specialized process that has documented procedures which are available for review. Solder balls cannot violate minimum electrical spacing. 100% verification of secured solder balls is required, sample verification is not allowed. Objective evidence for all solder balls accepted **shall** be maintained and be available for review. The specialized process and acceptance criteria **shall** be approved by the User prior to use.	''Solder balls and other metal particles'' was added to the first sentence. The second sentence was reworded and the remainder of the paragraph added to allow solder balls in certain controlled conditions using documented processes. Conductive particles can dislodge during ascent vibrations and float in micro-gravity environments causing short circuits.
8.3.2	**Flux Residues and Other Ionic or Organic Contaminants** Unless specified otherwise on engineering documentation approved by the User, cleanliness designator C-22 as described in the following paragraphs and the visual requirements for cleanliness (per 8.3) **shall** apply.	The published IPC J-STD-001D paragraph was replaced in its entirety to require that cleanliness designator C-22 is the minimum cleanliness level used for flight hardware.
9.1.10	**Measles** Measles **shall not** bridge noncommon conductors.	The requirement was reworded because: – the J-STD-001D published requirement is not inspectable – heritage data on government space programs shows that measles existing between, but not bridging, noncommon conductors do not present a reliability issue.
10	**Coating, Encapsulation and Staking (Adhesive)** a. A mix record **shall** be created for each mixed batch of multi-part polymers used for conformal coating, encapsulating, or staking. At a minimum, this record **shall** include the date mixed, manufacturer's part number and date/lot code, shelf-life expiration date (of all parts of the mix), and the mix ratio for all constituents used. b. For one-part polymers, the manufacturer's part number and lot/date code, and shelf life expiration date **shall** be documented. c. Materials **shall** be cured in accordance with the manufacturer's recommended cure schedule and within the thermal limitations of the hardware. Objective evidence of full cure for each batch of material **shall** be documented. A witness sample may be used for this verification. d. When coating, encapsulation, or staking materials are applied to through-hole glass, ceramic body, or hermetic components, the components **shall** be protected to prevent cracking, unless the material has been selected so as not to damage the components/assembly in its service environment. e. Equipment used for measuring viscosity, mixing, applying and curing silicone material **shall not** be used for applying other material. f. Prior to conformal coating, encapsulating, staking, the assembly and any fillers used (e.g., thickening agents, thermal property enhancers, etc) **shall** be treated to remove detrimental moisture and other volatiles. g. When fluorescent conformal coating materials are used, coverage and location **shall** be determined by UV-light examination. h. Areas to be coated, encapsulated, and/or staked **shall** be cleaned prior to material application.	Title changed to reflect addition of staking (adhesive) requirements. New paragraphs a - f added as new process requirements in four general categories: traceability, cure, part protection, and moisture removal.

J001D Reference	Space Applications Requirement (as changed by this Addendum)	Description of Change
10.1.1.2	**Conformal Coating on Connectors** Mating connector surfaces of printed circuit assemblies **shall** be free of conformal coating. The conformal coating specified on the assembly drawing(s)/ documentation should, however, provide a seal around the perimeter of all connector/board interface areas.	The first sentence was changed from ''...**shall not** be coated with conformal coating.'' to ''...**shall** be free of conformal coating.'' This change addresses both unintended application of coating on the mating surface, as well as the presence of coating for any other reason.
10.1.3 (New)	**Rework of Conformal Coating** Procedures which describe the removal and replacement of conformal coating **shall** be documented and available for review. Chemical stripping processes **shall** be approved by the User prior to use.	Rework of conformal coating was removed when J-STD-001 went from Revision C to Revision D (it will be addressed in the rework/repair series of IPC documents). Since reworking conformal coating can be destructive when not done properly, the requirement was carried over to this Space Addendum as new Clause 1.3.
10.2.2	**Performance Requirements** The applied encapsulant **shall** be completely cured, homogeneous, and cover only those areas specified on the assembly drawing(s)/documentation. The encapsulant **shall** be free of bubbles, blisters, or breaks that affect the printed wiring assembly operation or sealing properties of the encapsulant material. There **shall be no** visible cracks, crazing, mealing, peeling, and/or wrinkles in the encapsulant material. Minor surface swirls, striations, or flow marks are not considered defects.	To prevent unnecessary rework, a new last sentence was added allowing minor surface anomalies.

J001D Reference	Space Applications Requirement (as changed by this Addendum)	Description of Change
10.3	**10.3 Staking (Adhesive)** **a. Documentation** Components to be staked **shall** be identified on the assembly drawing(s)/ documentation. Some component packages should always be staked (e.g., solid-slug tantalum capacitors). Components identified as required to be staked on the assembly drawing(s)/ documentation **shall** be staked unless specified otherwise. **b. Placement** Staking materials **shall not** contact component lead seals unless the material has been selected so as not to damage the components/assembly in its service environment. **c. Unsleeved axial leaded components** Staking material **shall** be applied to both sides of the component. The length of the fillets of the staking material **shall** be minimum 50% to a maximum 100% of the length of the component. The minimum fillet height **shall** be 25% of the height of the component. The maximum fillet height **shall** be that the top of the component is visible for the entire length of the component. See Figure 10-1. **d. Sleeved axial leaded components** Staking material **shall** be in contact with both end-faces of the component and the surface it is being staked to. The minimum fillet height **shall** be at least 25% of the height of the component. The maximum fillet height **shall be no** greater than 50% of the height of the component, and **shall not** violate 10.3.b. See Figure 10-2. **e. Glass Bodied Components** Glass bodied components that are sleeved to protect them from possible damage caused by the staking material **shall** be staked in accordance with 10.3.c for unsleeved axial leaded components. **f. Radial leaded components whose longest dimension is their height (e.g., CKR capacitors, Single In-Line (SIP) resistor networks)** Individual components **shall** be staked in accordance with Figure 10-3. The staking material **shall** be applied to a minimum height of 25% to a maximum of 100% of the component body height. Closely spaced arrays consisting of up to four components **shall** be staked in accordance with Figure 10-4. Fillet height requirements for the two outer end-faces **shall** be the same as for an individual component. In addition, the top inner surfaces **shall** be bonded to each other for at least 50% of the components' width. Closely spaced arrays consisting of more than four components **shall** be staked in accordance with Figure 10-5. Staking **shall** be applied in the same manner as arrays up to four components, with the additional requirement that every other internal component **shall** have their sides staked to the board surface. **g. Radial leaded components whose longest dimension is their diameter or length (e.g., TO5 semiconductors, etc.).** Cylindrical components **shall** be staked in accordance with Figure 10-6. At least three beads of staking material **shall** be placed approximately evenly around the periphery of the component. For each bead, the staking material **shall** contact a minimum-25% to maximum-100% of the height of the component body. Slight flow of staking material under the component body is acceptable provided it does not violate 10.3b. Rectangular components **shall** be staked in accordance with Figure 10-7. A bead of staking material **shall** be placed at each corner of the component. For each bead, the staking material **shall** contact a minimum-25% to maximum-100% of the height of the component body. Slight flow of staking material under the component body is acceptable provided it does not violate 10.3b. **h. Fasteners** Fasteners identified on the drawing to be staked **shall** be staked either: • At two places spaced approximately opposite of each other. Each bead of staking material **shall** cover at least 25% of the perimeter of the fastener in accordance with Figure 10-8. • One bead of staking material that covers at least 50% of the perimeter of the fastener in accordance with Figure 10-9.	New section for staking (adhesive) requirements.

J001D Reference	Space Applications Requirement (as changed by this Addendum)	Description of Change
10.3.1	**Staking shall**: a. Be completely cured and homogeneous. b. Be free of voids or bubbles that expose component conductors, bridge noncommon conductors and/or violate design electrical clearance. c. Not bridge between the substrate and the bottom of radial leaded components. This does not apply to bonding or underfilling when used as part of a documented process. d. Be free of contamination. e. Not negate stress relief.	New section for staking (adhesive) requirements.
10.3.2	**Staking Inspection** Visual inspection of staking may be performed without magnification. Magnification from 1.75X to 4X may be used for referee purposes.	New section for staking (adhesive) requirements.
11.2.2	**Visual Inspection** After the soldering and cleaning process is complete, all assemblies **shall** be evaluated by 100% visual or nondestructive inspection (see 1.11) except for solder connections as specified in 4.14.4 and 7.6.14. When assemblies are to be conformally coated and/or staked or encapsulated, the coating, encapsulation, and/or staking **shall** be evaluated by 100% visual inspection. If the presence of a defect cannot be determined at the inspection power, the item is acceptable. The referee magnification power is intended for use only after a defect has been determined but is not completely identifiable at the inspection power.	The first sentence was reworded to require 100% visual or nondestructive inspection. The change, in effect, disallows sampling inspection plans because SPC is difficult to apply to low volume production runs.
11.2.3, some of 11.3	Disregard these paragraphs which provide for sampling inspection.	Adequate sampling plans are difficult to apply to low volume production runs.
Appendix A	Add as a Note Appendix A: All additional defects identified by this space addendum **shall** be considered part of Appendix A.	Appendix A cannot realistically be recreated in this addendum. The Note is added to classify any departures from the requirements added by this Addendum as defects.

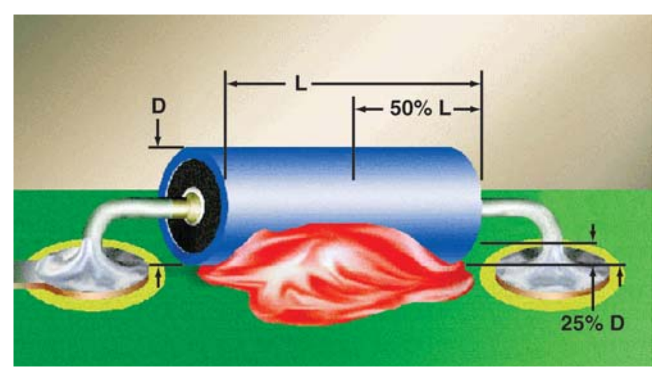


Figure 10-1

Acceptable (see 10.3.c)

- Fillet Length: 50%L to 100%L
- Fillet Height: 25%D to 100%D. Top of component is visible for its entire length.

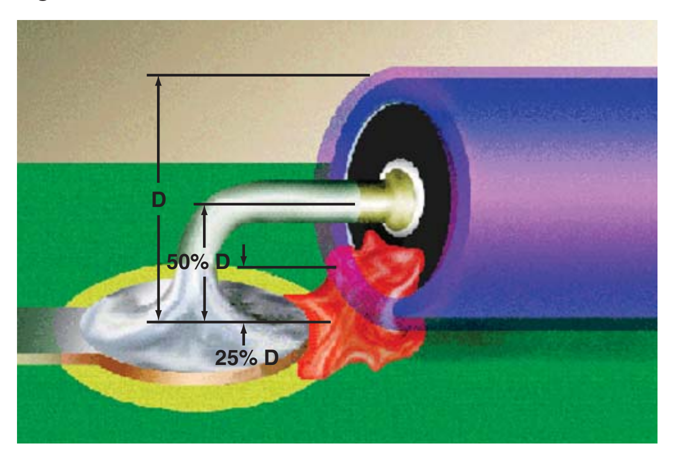


Figure 10-2

Acceptable (see 10.3.d)

- Staking is in contact with both end-faces of component.
- Fillet Height: 25%D to 50%D and does not contact lead seals or solder termination.

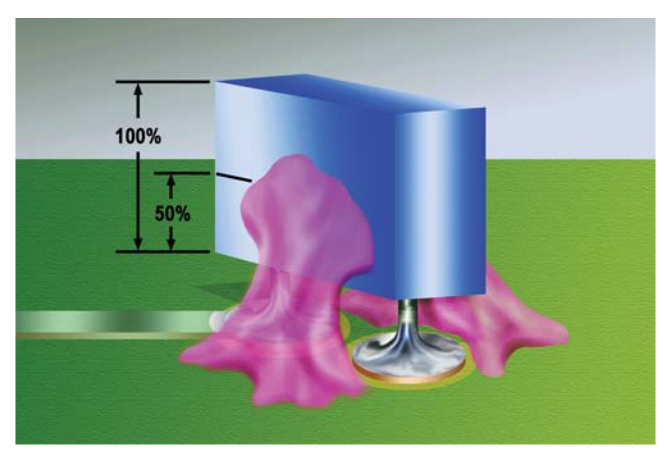


Figure 10-3

Acceptable (see 10.3.f)

• Fillet Height: 25%H to 100%H.

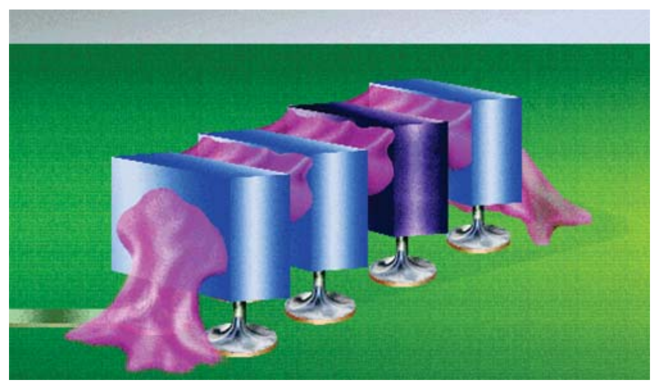


Figure 10-4

Acceptable (see 10.3.f)

• Two outside ends - fillet height: 25%H to 100%H.

• Inner surfaces - fillet is in contact with both surfaces for 50% of component width.

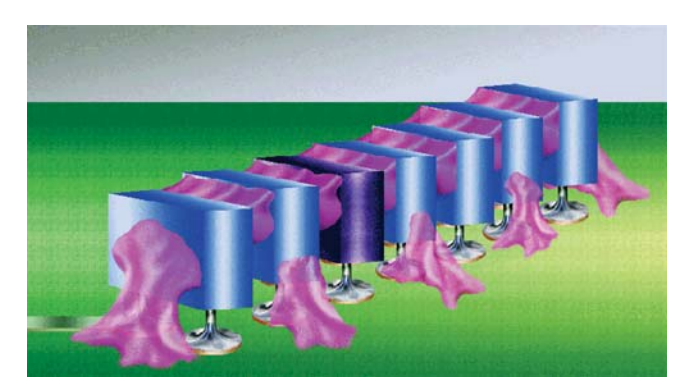


Figure 10-5

Acceptable (see 10.3.f)

• Two outside ends - fillet height: 25%H to 100%H.

• Inner surfaces - fillet is in contact with both surfaces for 50% of component width.

• Side of every other internal component is staked to board surface.

Acceptable (see 10.3.g)

- At least three beads spaced approximately evenly around periphery of component.
- Each bead fillet height 25%H to 100%H.
- Slight flow underneath component, but bead(s) do not contact lead seals or solder termination.

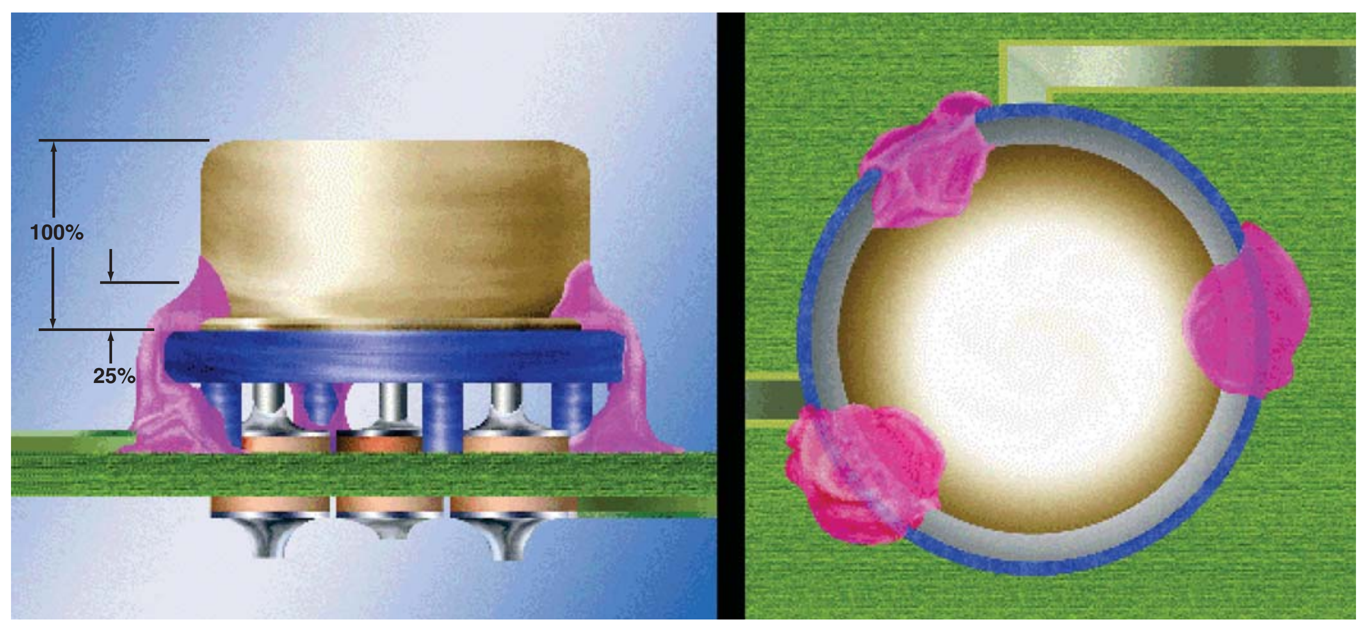


Figure 10-6

Acceptable (see 10.3.g)

- A bead of staking material at each corner.
- Each bead fillet height 25%H to 100%H.
- Slight flow underneath component, but bead(s) do not contact lead seals or solder termination.



Figure 10-7

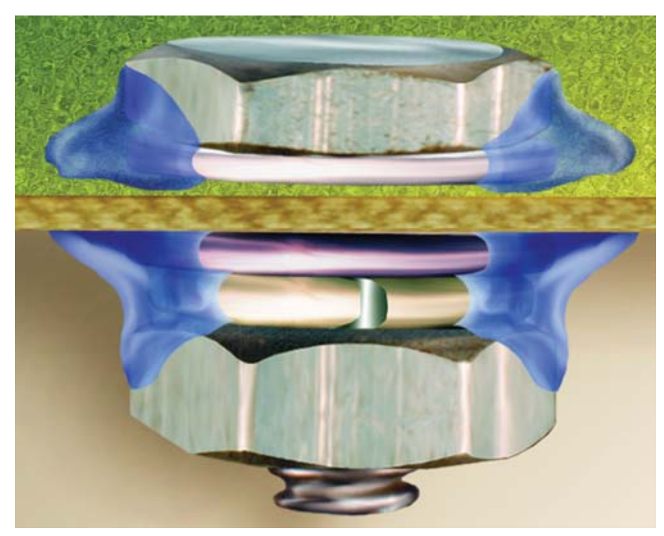


Figure 10-8

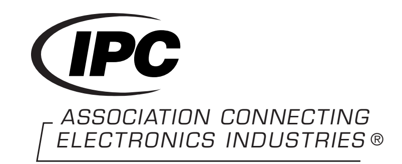
Acceptable (see 10.3.h)

- Two beads of staking material placed approximately opposite of each other.
- Each bead of staking material is at least 25% of the perimeter of the fastener.

Figure 10-9

Acceptable (see 10.3.h)

- One bead of staking material that covers at least 50% of the perimeter of the fastener.



Standard Improvement Form

IPC J-STD-001DS

The purpose of this form is to provide the Technical Committee of IPC with input from the industry regarding usage of the subject standard.

Individuals or companies are invited to submit comments to IPC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

IPC
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Bannockburn, IL 60015-1249
Fax 847 615.7105
E-mail: answers@ipc.org

---

1. I recommend changes to the following:

___ Requirement, paragraph number __________

___ Test Method number __________, paragraph number __________

The referenced paragraph number has proven to be:

___ Unclear ___ Too Rigid ___ In Error

___ Other ____

---

2. Recommendations for correction:

____

____

____

____

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3. Other suggestions for document improvement:

____

____

____

____

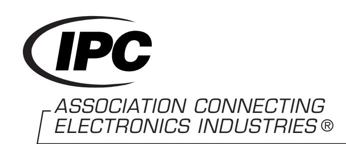
Submitted by:

Name ______________________________ Telephone ______________

Company ______________________________ E-mail ______________

Address ____

City/State/Zip ______________________________ Date ______________



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